PATENT ABSTRACTS OF JAPAN

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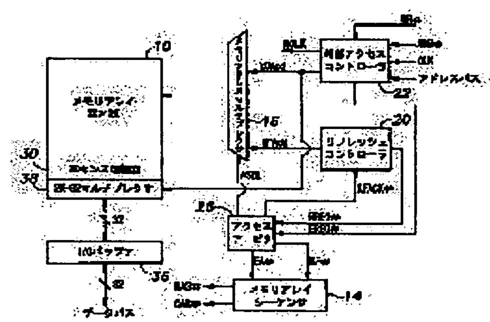
(54) METHOD AND APPARATUS FOR 1-TSRAM COMPATIBLE MEMORY

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain an SRAM compatible memory using DRAM cells which never delay in an external access due to refresh by judging whether the external access to a memory array is processed and if the external access is processed, executing the refresh.
SOLUTION: Upon detection of an external access, an external access controller 33 makes a request signal EREQ2970 active for an access arbiter 26, and the access arbiter 26 sets an ASEL signal high to select an address on an external access address bus ECAdd for an accessing address to the memory array 10. If the external access conflicts with an access to refresh, the access arbiter 26 gives access priority usually to the external access and hence the external access never delays due to refresh.



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CLAIMS

[Claim(s)]
[Claim 1] The process in which are an approach for operating a memory array equipped with two or more memory cells which need to be refreshed periodically, and it judges whether external access to said memory array is unsettled, The approach characterized by having the process in which said external access is performed when judged with external access being unsettled, the process in which it judges whether refresh is unsettled, and the process in which said refresh is performed when judged with external access not being unsettled.
[Claim 2] The approach according to claim 1 characterized by having further the process which accumulates all refreshes that were not performed while external access was unsettled in order to perform said refresh behind.
[Claim 3] The approach according to claim 1 characterized by equipping said each cel with one transistor.

[Claim 4] The approach according to claim 1 characterized by said each cel being a DRAM cel.
[Claim 5] The approach according to claim 1 characterized by said memory array having peak clock frequency equal to the peak frequency of said external access at least.
[Claim 6] The approach which is an approach for operating a memory array equipped with two or more memory cells which need to be refreshed periodically, and is characterized by having the process in which it judges whether refresh is unsettled, and the process in which said unsettled refresh is performed only throughout at the time of the idle during external access to said memory array.
[Claim 7] The memory system characterized by being a memory system, having the array of the memory cell which needs to be refreshed periodically, the access controller connected to said memory array in order to access said memory cell from the outside, and the refresh controller connected to said memory array since said memory cell is refreshed, and refreshing said refresh controller for said memory cell only throughout at the time of the idle during external access to said memory cell.
[Claim 8] The system according to claim 7 characterized by having further the arbiter connected between said access controllers and said refresh controllers.
[Claim 9] The system according to claim 7 characterized by each memory cell being a DRAM cel.
[Claim 10] The system according to claim 7 characterized by equipping said memory cell with one transistor, respectively.
[Claim 11] The system according to claim 7 characterized by said memory array having peak clock frequency equal to the peak frequency of said external access at least.
[Claim 12] The system according to claim 8 characterized by having further the accumulator formed in said refresh controller in order to accumulate said refresh until refresh comes to be performed throughout at the time of said idle.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to semiconductor memory. In order that this invention may assemble SRAM compatibility memory in relation to both SRAM and DRAM in a detail, it relates to using a DRAM cel.
[0002]
[Description of the Prior Art] the conventional DRAM (dynamic random access memory) memory cell which consists of one transistor (1-T) and one capacitor has remarkably small chip surface area, and, so, it is cheaper than the SRAM (static random access memory) cel which is alike as usual and consists of 4-6 transistors. However, the data stored in a DRAM cel do not have the need to refreshing periodically in a SRAM cel. Although the conventional technique SRAM, for example, false ["false" (refer to Toshiba data book in 1990)], tried to use a DRAM cel for SRAM application, it was almost ineffective, and since the external signal was needed in memory refresh in order that the device might control memory refresh, delay was produced in external access. As a result, refresh does not have permeability and the device does not have compatibility with a SRAM device in essence.
[0003]
[Problem(s) to be Solved by the Invention] It is offering the SRAM compatibility memory using the DRAM cel which the delay in external access does not produce by refresh.
[0004]
[Means for Solving the Problem] The single transistor memory cell according to this invention is the same as the conventional DRAM cel in general. Therefore, the memory needs periodic refresh. Refresh occupies memory bandwidth. If the total bandwidth generally needed by both refresh and external access is below the memory bandwidth given by the memory cell array, in external access, memory refresh is completely (related with timing) uninfluential, and can be performed. Since refresh is a comparatively rare event, the average bandwidth which refresh occupies is relatively small compared with available peak bandwidth to a memory array. For example, in the case of one example of this invention, memory clock frequency is 100MHz and the refresh frequency (in the case [Being the memory cell of 1000 lines.] of each end-of-a-road 16msec refresh time amount) of 62.5kHz is occupied 0.0625% of full-available bandwidth.
[0005] Theoretically, if an external access frequency is 99.9375MHz, refresh will not affect it at all about external access. However, in fact, when the cycle time of a memory array is 10ns, generating of each refresh access takes 10ns, and each external access takes at least 10ns. In order to perform refresh to transparency to external access, the external access time takes 20ns (it is 10ns to 10ns and actual access to refresh), namely, the external access frequency should become smaller than 50MHz. Refresh is the frequency which is 62.5kHz and supporting that 50MHz application performs refresh using a 100MHz memory array does not have it. [economical] Still more generally the average frequency of external access is smaller than a peak access frequency. There is almost nothing that has a utilization factor (an average frequency / peak frequency) exceeding 99.9% with an existing memory system in fact. Therefore, peak clock frequency can be equal to a peak external access frequency, or can be slightly large, memory refresh can be performed using a low average access frequency, and the memory system using a 1-T cel make it the memory system appear as SRAM can be designed.
[0006]
[Embodiment of the Invention] In the one example of this invention, a memory cell array has 32-bit 128K WORD. So, the array has 32 data I/O line. Drawing 1 shows an example of this memory system which

has such an array. A memory system equips the memory cell array 10, the memory array sequencer 14, the memory address multiplexer 16, the refresh controller 20, and external access controller 22 list with the access arbiter 26. A memory array 10 is arranged in 2K lines and 2K train. The sense amplifier in block 30 which performs write-in actuation in data sensing and a restoration list relates to each train. One cel array line is made into operating state during each access, and 2K memory cell of the line is connected to the sense amplifier 30 within each train.

[0007] a sense amplifier 30 is boiled as usual and connected to I/O buffer 36 through the 2K-32 train multiplexer 38 of a lot. The memory array sequencer 14 generates DRAM control signal RAS# as usual and CAS#, in order to control actuation of an array. The function of RAS# and a CAS# signal is the same as the function indicated by U.S. Pat. No. 5,615,169 by the same artificer, is referred to here and is using the whole as some of these specifications. The external access controller 22 interprets an external access command, and generates read-out/write request. In the one example, external access is decided using two signals. The signal is a clock (CLK) and an address SUSUTO lobe (ADS#). External access is detected by the start clock edge in the operating state of an address strobe (ADS#) signal.

[0008] Drawing 2 shows the timing relationship of these two signals. Signaling of ADS# and CLK is the same as that of the industry standard in synchronous [SRAM] (for example, please refer to Intel Pentium Processor 3.3 v Pipelined BSRAM specification version 2.0 as of March 25, 1995).

[0009] In the another example, an external-interface signal can be made to be the same as that of a standard signal asynchronous [SRAM] (please refer to the data sheet for Mitsubishi Semiconductor Memory Data Book, M5M5178P, and 64KSRAM in 1990). An ADS# signal can be internally generated by the same address transition detector as what is indicated by in this case, November, 1991 JSSC by Murakami etc., Vol.126, No.11, and pp.1563-1567"A 21-mW 4-Mb CMOS SRAM for Battery Operation." Therefore, the generated ADS# signal can be used in order to make it synchronize with the interior action of memory.

[0010] At the time of detection of external access, the external access controller 22 makes operating state demand signal EREQ# to the access arbiter 26, and the access arbiter 26 makes an ASEL signal a high, and it chooses the address on the external access address bus ECAdd for the address for access to a memory array 10. Moreover, an arbiter 26 also makes operating state the external access EA# signal inputted into the memory array sequencer 14 which generates RAS# and CAS# for controlling array actuation. The timing of these signals is also shown in drawing 2 .

[0011] When access between external access and refresh collides, an access priority is usually given by the arbiter 26 to external access. By doing so, external access does not produce delay by refresh. This example is formed so that it may have memory cycle time amount equal to a clock period, therefore it makes possible random access for every clock cycle. The access can be random, namely, the access can be the address of the arbitration which spreads to device address space. It is at the initiation time of a clock cycle, and an arbiter 26 evaluates the demand, drives the ASEL signal inputted into the address multiplexer 16, and chooses one of the two addresses. The two addresses are a refresh address RFAdd or the external access address ECAdd, and are used for actuation of a memory array 10. Refresh access comes to be performed by the arbiter 26 only when external access does not exist. Refresh is delayed when a collision takes place. This timing is also shown in drawing 2 .

[0012] The refresh controller 20 generates a refresh demand periodically so that it may ensure that a memory array 10 is refreshed suitably. Since it refreshes between the refresh time amount for 16ms when there is a memory array 10, the refresh controller 20 generates one refresh demand every 8 microseconds. Refresh demand signal RREQ# is made into operating state when unsettled refresh exists. The operating state of a RREQ# signal is detected by the arbiter 26 with the start edge of a MCLK signal. When an external access request is not detected, an arbiter 26 makes both refresh discernment RFACK# and an ASEL signal the low between one clock cycles. It is used for refresh of a current memory cycle, and a subsequent memory cycle chooses the refresh address from the refresh controller 20 as the address to a memory array 10.

[0013] Drawing 3 is the block diagram of the refresh controller 20, and equips the refresh address counter 40 and refresh timer 44 list with the refresh accumulator 50. The refresh counter 40 gives a 11-bit line address to a memory array 10 into a refresh cycle. The increment of the refresh counter 40 is carried out at the time of the termination of a refresh cycle in which signaling is carried out by halt of refresh discernment RFACK# of operation. The refresh timer 44 is reset at the time of starting (reset signal). A timer 44 is equipped with 12 bit counters 46 which realize all the counts of 4095 cycle, and 12 input NAND gate 48. In the case of 100MHz clock frequency, the deadline of a timer 44 is passed every about 8 microseconds (signal Q0-Q12 become a high).

[0014] When all counter bit Q0-Q12 become a high, a refresh rise RFUP# signal is made a low by NAND gate 48 between one clock cycles. This signal is inputted into the refresh accumulator 50 in order to increment triplet rise / down counter 52. An updown counter 52 increments only 1, when RFUP# is made into a low, and when RFACK# is made into the low between one clock cycles, it carries out the decrement only of 1. A counter 52 stops an increment, when becoming full count (i.e., when AQ0-AQ2 becomes a high altogether). When accumulator 50 count is not empty (i.e., when signal AQ0-AQ2 is not 000), the refresh demand RRQg is made a low by the OR gate 54. The function of an accumulator 50 is shown below.
[0015] External access between one or the refresh deadline periods beyond it (respectively about 8 microseconds) may continue. In this case, in order to adjust without losing a refresh cycle, a refresh demand is accumulated in an accumulator 50. The refresh demand RREQ# signal over an arbiter 26 is made into a low state until an accumulator 50 becomes empty. In this example, an accumulator 50 can be accumulated up to 7 refreshes. Thereby, the system can continue external access between the periods by 56 microseconds, without losing a refresh cycle. Generally in the computer system aiming at this typical memory system functioning, continuous external access longer than 56 microseconds is not generated (in other applications, the magnitude of a counter 52 can be fluctuated so that that requirement for application may be satisfied).
[0016] in this example, from the external clock signal CLK, the signal MCLK which synchronizes with actuation of a memory system is boiled as usual, and is drawn. MCLK can make it generate by a conventional oscillator on chip and PLL (phase locked loop) in the another example. PLL synchronizes with the MCLK start edge to the output of an address transition detector, and an address transition detector generates a pulse, in case transition occurs on an address bus.
[0017] Drawing 4 shows an example of the internal structure of the arbiter 26 of drawing 1 , and is equipped with NAND gate 56 connected to an inverter 58 so that it may be illustrated by this example. In this way, refresh is prevented except for the case where unsettled memory array external access does not exist.
[0018] This indication is a thing for instantiation and is not restricted. Still more nearly another example of modification is clear to this contractor from a viewpoint of this indication, and it is the thing by which the example of modification also goes into an attached claim and which carries out a thing intention.
[0019]
[Effect of the Invention] By this invention, the SRAM compatibility memory using the DRAM cel which the delay in external access does not produce by refresh can be offered.

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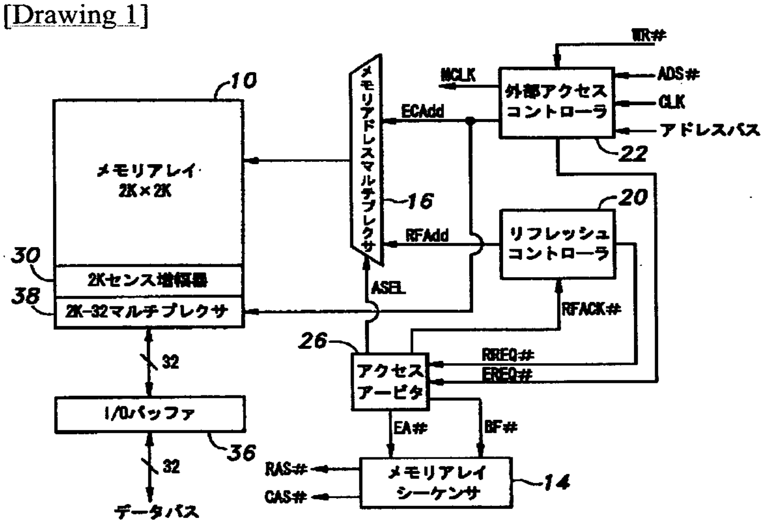
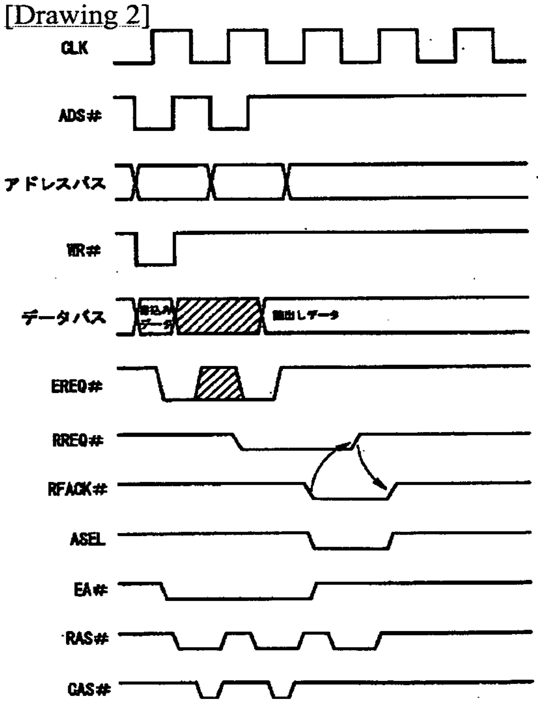
DRAWINGS

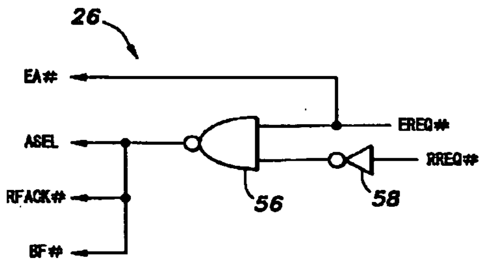
[Drawing 1]



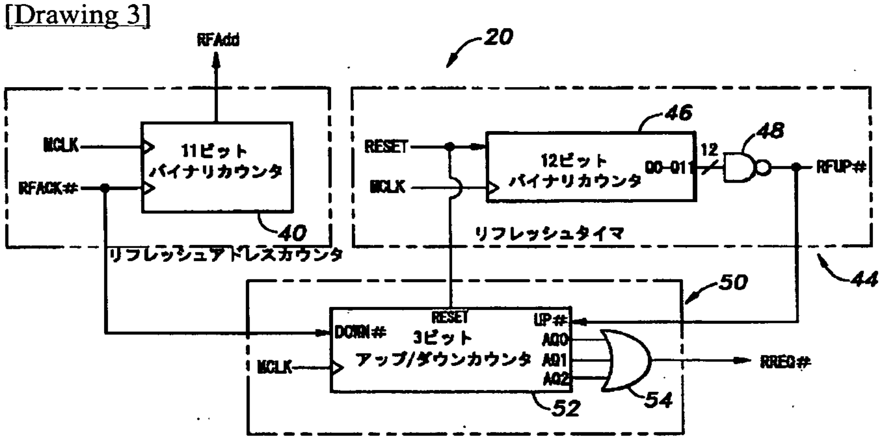
[Drawing 2]



[Drawing 4]



[Drawing 3]



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